COMPLETE LISTING OF CLAIMS IN ASCENDING ORDER WITH STATUS INDICATOR

1. (Currently amended) An image sensor, comprising:

an image acquisition portion;

an image processing portion, receiving image information from said image acquisition portion, said image processing portion including a CMOS circuitry with CMOS differential outputs having an output impedance; and

an image receiving portion, having an input impedance, receiving said image information from said CMOS outputs, said image processing portion producing a current mode output and said image receiving portion receiving said current mode output; and

an impedance matching device, matching said output impedance of said image processing portion to said input impedance of said image receiving portion.

2. (Original) A sensor as in claim 1 wherein said image processing portion includes a portion with a CMOS output.

3. (Original) A sensor as in claim 1 wherein said impedance matching circuit comprises a circuit on said image processing circuit.

4. (Currently amended) A sensor as in claim 3 wherein an output circuit of said image processing circuit includes a ~~current biased~~ transistor adapted to receive a current bias, wherein a magnitude of the current bias sets the output impedance.

5. (Original) A sensor as in claim 4 wherein said output impedance is matched to an input impedance of the image receiving circuit.

6. (Original) A sensor as in claim 1 wherein said impedance matching circuit comprises a circuit on said image receiving circuit.

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7. (Currently amended) A sensor as in claim 6 wherein an input circuit of said image receiving circuit includes a ~~current biased~~ transistor adapted to receive a current bias, wherein a magnitude of the current bias sets the input impedance.

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8. (Original) A sensor as in claim 4 wherein said input impedance is matched to an output impedance of the image processing portion.

9. (Original A sensor as in 1 wherein said impedance matching circuit comprises a first circuit on said image processing circuit and a second circuit on said image receiving circuit.

10. (Currently amended) A sensor as in claim 9 wherein said first and second circuits include ~~current biased~~ respective elements adapted to receive respective current biases, and wherein ~~a magnitude~~ respective magnitudes of the current ~~bias sets~~ biases set the respective output ~~impedance~~ impedances.

11. (Original) A sensor as in claim 4 wherein said output impedance of said image processing circuit is matched to an input impedance of the image receiving circuit.

12. (Original) A sensor as in claim 1, wherein said image receiving circuit includes a current mirror part, that mirrors an input current.

13. (Original) A sensor as in claim 1 wherein said image acquisition circuit is an active pixel sensor with a photosensor, an in-pixel buffer, and an in pixel select transistor.

14. (Currently amended) A sensor as in claim 13 wherein said ~~an~~ image acquisition portion and said image processing portion operates at substantially zero voltage.

15. (Currently amended) An image sensor, comprising:

an image acquisition portion;

an image processing portion, receiving image information from said image

acquisition portion at a differential input; and

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an impedance matching device, matching ~~said~~ an output impedance of said image ~~processing~~ acquisition portion to ~~said~~ an input impedance of said image ~~receiving~~ processing portion by adjusting bias current through at least one biased device in a way that renders ~~the~~ said input impedance relatively independent of an input current.

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16. (Original) An image sensor as in claim 15, wherein said image acquisition portion and said image processing portion each operate in current mode.

17. (Currently amended) An image sensor as in claim 16, wherein said ~~portions~~ image acquisition portion and said image processing portion operate at substantially zero voltage.